

Appl. No. 09/884,675  
Amdt. dated September 17, 2004  
Reply to Office action of June 30, 2004

**Amendments to the Specification:**

Please replace the title with the following amended title:

~~Hardware Efficient Handling Of Instruction Exceptions To Limit Adverse Impact On Performance~~  
Method and System With Multiple Exception Handlers In A Processor.

**Please replace paragraph [0029] with the following amended paragraph:**

**[0029]** According to the preferred embodiment, a multiplexer 175 or other similar circuit or logic combines the potential output from the two handlers 125, 150 onto a single set of wires to minimize the circuitry required to respond to the exception handlers 125, 150. Thus, according to the preferred embodiment, the multiplexer 175 selects one of the selected exceptions from handlers 125, 150 and signals other parts of the processor to indicate that an exception has arisen that is ripe for resolution, or which has been already resolved. ~~As will be apparent to one skilled in the art, a~~ variety of different multiplexing schemes may be used to determine which exceptions to select from the handlers 125, 150. Moreover, it is possible that different multiplexing decisions may be implemented in the same system, based on various operating conditions or parameters. Generally, according to the preferred embodiment, the default condition of the multiplexer 175 is to select the non-critical exceptions selected by non-speculative exception handler 125, if such an exception appears at the output port of the non-speculative exception handler 125. The non-speculative exception is chosen since it is guaranteed to be an exception from the actual program flow. If no excepted instruction is provided at the output port of the non-speculative exception handler 125, the multiplexer 175 selects the excepted instruction appearing at the output port of the speculative exception handler 150. According to one embodiment, the multiplexer 175 may be configured to periodically select the speculative handler 150 even in the event that an exception is pending at the output port of the non-speculative exception handler 125 to ensure that the speculative exception handler 150 does not become starved. As yet another alternative, various other arbitration schemes may be used to

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determine how the exceptions are selected from the exception handlers 125, 150, with the understanding that one of the primary criteria is that handling of critical exceptions is generally expedited, while non-speculative exceptions are guaranteed to be from the actual program path. As yet another embodiment, the multiplexer 175 may be omitted, and separate lines may extend from each exception handler 125, 150 to the rest of the processor circuitry. In this event, redundant circuitry may be required in the processor circuitry to handle the dual output ports from the exception handling section 100.